I3C Interop Workshop Draft Plan

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I3C Interop Workshop

- The I3C and I3C Basic Working Groups are hosting a MIPI I3C Interop Workshop in conjunction with the upcoming Member Meeting, and all MIPI members and nonmembers are invited to participate. The event will offer the opportunity for implementers of MIPI I3C, I3C Basic and I3C HCI to engage in interoperability testing between Controller and Target devices in a confidential environment protected by non-disclosure agreements (required for event access).

I3C Interop Workshop

Objective: To offer an opportunity for I3C implementers to participate in initial to advanced interoperability testing. MIPI Contributors and Adopters are invited to join.

Platform: Standardized cabling (.1 inch spacing – female-female wires, GND, SDA, GND, SCL, GND). Legacy I2C device allowed (may be provided by Bosch). Power supply may be needed for Targets. 1.8v and 3.3v devices present.

Features under Test:

- Pure and Legacy I3C SDR Read/Write
- I3C SDR Read/Write
- Dynamic Address Assignment **(including SETDASA and RSTDAA)**
- IBI with/without MDB – if supported
- Basic Direct CCC's
- Enter/Exit HDR (for SDR only devices)
- DDR Read/Write/CRC – if supported
- TSP Read/Write – if Target supported
- Controller/Target Error Handling
- Multi-Target Topologies (at least two I3C devices) – After confirmed point-to-point functionality
  - Include Direct/Broadcast CCC's
- HCI v1.0 related tests – to ensure a hardware and standard software compatibility
- Timing Control
  - Sync Mode
  - Async Mode 0/1 and Async Mode Exit
- Secondary Controller/Main Controller Handoff – if supported
- Target Reset
- Multilane features
- 1.2V support for devices that are supporting it
- Group Addressing
- Any other I3C v1.1.1 and I3C Basic v1.1.1 capabilities supported

Test Equipment: Tektronix can provide two o-scopes with I3C protocol Trigger and Decode analysis and active probes.

Anticipated Test Matrix: Approximately **tbd** controllers X **tbd** Targets

Other: Device Characteristics Register (DCR) assignments are available for each I3C Target

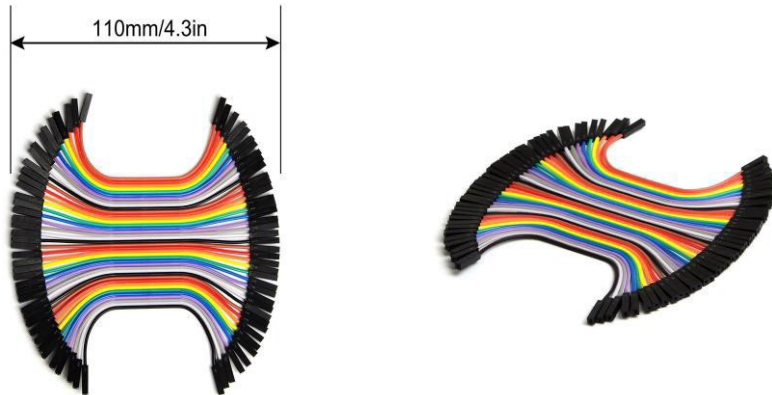mipi alliance

Physical Interface

Objective: Maintain a consistent physical interconnect of design and length for easy interoperation between varied test PCBs and typical I3C functionality

Design: 0.1 inch spacing female to female AWG 26 ribbon cable with solderless individual connectors.

Pinout: GND, SDA, GND, SCL, GND

Length: Max 15cm (0.02Ohm, 2.5pf)

Example: https://www.amazon.com/dp/B01L5ULRUA?psc=1

110mm/4.3in

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Conformance Test Suite for I3C/I3C Basic v1.1.1

- A conformance test suite (CTS) has been developed to improve the interoperability of products that adopt the MIPI I3C® interface. It defines a set of conformance or interoperability tests whereby products can be tested against other implementations of the I3C or I3C Basic v1.1.1 specifications.

- This first version of the CTS is limited to meet time-to-market requirements imposed by the rapid adoption of I3C in the marketplace. Given this, the I3C Working Group has decided to focus this version of the CTS on the following:

  - SDR-only devices without optional I3C capabilities

  - All controller and target error detection and recovery methods

  - Basic HDR Enter/Tolerance/Restart/Exit in scope, but HDR-DDR under consideration

- CTS is available here - https://www.mipi.org/specifications/i3c-sensor-specification

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Proposed Room Layout (TBD)

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